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BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte SAMEH S. REZEQ, ROBERT B. STASZEWKI,
and KURRAM MUHAMMAD

Appeal 2007-3823
Application 10/821,487
Technology Center 2800

Decided: April 11, 2008

Before ROBERT E. NAPPI, JOHN A. JEFFERY,
and CARLA M. KRIVAK *Administrative Patent Judges.*

NAPPI, *Administrative Patent Judge.*

DECISION ON APPEAL

This is a decision on appeal under 35 U.S.C. § 6(b) of the final rejection of claims 1 through 28.

We affirm the Examiner's rejections of these claims.

INVENTION

The invention is directed to making sigma-delta modulators faster by splitting the accumulators of the modulator into parallel chains of accumulators. See page 3 of Appellants' Specification. Claim 1 is representative of the invention and reproduced below:

1. A sigma-delta modulator, comprising:

a lower-order accumulator chain configured to process only lower-order bits of an input number;

a higher-order accumulator chain configured to process only higher-order bits of said input number; and

a combiner coupled to both said lower-order and higher-order accumulator chains and configured to align results therefrom to generate output bits of a given order.

REFERENCE

Kimura	US 5,079,551	Jan. 7, 1992

REJECTION AT ISSUE

Claims 1 through 28 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Kimura. The Examiner's rejection is on pages 2 and 3 of the Answer.

Throughout the opinion, we make reference to the Brief (received February 17, 2006) and the Answer (mailed March 9, 2006) for the respective details thereof.

ISSUES

Whether Appellants have shown that the Examiner erred in rejecting of claims 1 through 28 under 35 U.S.C. § 103(a).

PRINCIPLES OF LAW

"Once the PTO has made an initial determination that specified claims are not patentable (the prima facie case concept, *see In re Oetiker,* 977 F.2d 1443, 1448 (Fed.Cir.1992)), the burden of production falls upon the applicant to establish entitlement to a patent. *See In re Spada,* 911 F.2d 705,

708, (Fed.Cir.1990); *In re King,* 801 F.2d 1324, 1327 (Fed.Cir.1986) (burden shifts to appellant after the PTO establishes a *prima facie* case of anticipation)." *In Re Morris* 127 F.3d 1048, 1054 (Fed. Cir. 1997)

ANALYSIS

Appellants' arguments on page 7 of the Brief, are directed to claims 1 through 28 as a group. Thus, in accordance with 37 C.F.R. § 41.37 (c)(1)(vii) we group claims 1 through 28 together and select claim 1 as representative of the group.

Appellants' entire argument on appeal is as follows:

> Claim 1 includes a lower-order accumulator chain for processing only lower order bits and a higher-order accumulator chain for processing only higher-order bits. The references of record do not show, teach, or suggest these limitations. The Kimura reference does not show, teach, or suggest the accumulator chains of Claim 1. U.S. Patent No. 5,079,551 discloses an addition circuit for adding feedback digital data to input data. U.S. Patent No. 5,079,551 does not show accumulator chains.

Brief 7.

In response, the Examiner states on pages 3 and 4 of the Answer:

> The remarks filed in the brief again concede that Kimura's circuit adds feedback data to input data, but refuses to accept the Kimura circuit as an accumulator. While Kimura et al. may not use the term accumulator a brief study of Kimura figure 1 reveals that the addition circuit adds feedback data which had been in the feedback path sample delay to the input data and again latches this in the feedback path latch, which meets the definition of accumulation. Kimura also separates the bits by significance (DO-D7 & D8-D15), i.e. low order and high order, and has separate adders for the lower order bits and higher order bits and the accumulation for the respective lower order and higher order bits appears separate as can be seen in the numbering of the lines provided between the adders (34,

> 40; fig. 1) and the latches (36, 46; fig. 1) to indicate the number of result lines. Carry bits from the adders/accumulators are passed up from the lower order chain to the higher order chain (delays 38, 48; fig. 1) and from the higher order accumulators to the output combiners (adders 56, 60, 62; fig. I). Kimura also discloses plural adders/accumulators connected together for both the high order and low order bits. The first accumulator for the lower order chain of accumulators is provided by adder 34 which receives and adds the eight bits of lower order input data D7-DO and eight bits of data from delay 36; the sum is passed back to the delay 36 with a carry bit, if generated, passed up to the high order chain. The sum is also fed to the next accumulator stage (adder 45). A similar arrangement is provided for the first accumulator of the high order accumulator chain --adder 40, delay 36 and carry bit to delay 46. The high order accumulator has a delay stage 32 at the input in order to match the timing, i.e. give the low order stage an opportunity to get its result.

The Examiner made similar findings in the September 20, 2005 Final Office Action.

Appellants' arguments have not persuaded us that the Examiner erred in rejecting claims 1 through 28 under 35 U.S.C. § 103(a). The Examiner has established a *prima facie* case based upon a well reasoned explanation of how the high order and low order adders of Kimura meet Appellants' claimed high and low order accumulators. Appellants have not explained why the Examiner's finding is in error and why the adders in Kimura's device do not function as the claimed accumulator chains. Thus, we do not find that Appellants have carried the burden of proving that the Examiner erred in rejecting claim 1 or the claims grouped with claim 1. Accordingly, we sustain the Examiner's rejection of claims 1 through 28 under 35 U.S.C. § 103(a).

CONCLUSION

We affirm the Examiner's rejections of claims 1 through 28.

ORDER

The decision of the Examiner is affirmed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv).

AFFIRMED

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